SECTION XXIII

TELECOMMUNICATIONS FRAMED E1 OUTPUT (OPTION)

March 25, 1998

1-1 INTRODUCTION

1-2 The 87-6000-E1 option provides the user with telecommunications timing signals meeting the requirements of ITU-T G.703 and ITU-T G.704 for the 16-Frame Multiframe. In addition, when the host XL-DC is configured with an appropriate high stability oscillator option, the requirements of ANSI T1.101-1994 and ITU-T G.811 pertaining to Primary Reference Source operation may be met.

1-3 This option consists of a single height or double height (depending upon optional output configuration) plug-in module. In the standard single height configuration, all output signals are balanced and provided on panel mounted wire-wrap pins. The optional double height panel configuration provides unbalanced outputs on BNC connectors in addition to the balanced E1 signals available on the wire-wrap pins. In both configurations, two sets of Form-C relay closures are also included for major and minor alarm indications. These closures are accessible on panel mounted wire-wrap pins.

1-4 SPECIFICATIONS

1-5 This module may be configured to provide an assortment of outputs. The standard configuration provides:

Framed All 1's CEPT E1 2048 Kb/S Outputs (Two Outputs)

Format:	16 Frame Multiframe.
Line code:	HDB3/AMI (these are the same for all 1's).
Interface:	Balanced, Z_0=120 Ω, on wire wrap pins. Unbalanced, Z_0=75 Ω, on BNC connectors.
Wave Shaping:	CEPT G.703 pulse template requirements.
AIS:	User may enable assertion of Alarm Indication Signal (AIS) on occurrence of a major fault, via DIP switch setting.

Major and Minor Alarm Relay Closures

Format:	Form-C Normally Open and Normally Closed contacts available on panel mounted wire wrap pins.
Contacts:	Rated to 115 VAC/150 VDC at 2 A.

In addition to the E1 outputs and Alarm relay closures, up to four optional outputs may be provided. These are factory configured from these options:

64 Kb/s Composite Clock Output

Format:	As per ITU-T G.703 Centralized Clock Interface, para. 1.2.2. AMI with 5/8 duty cycle. All 1's with Bipolar Violations at an 8 Kb/s rate.
Interface:	Balanced, 2 V peak into 135 Ω, on wire wrap pins.
Alarm Control:	Output may be user configured to be turned off on occurrence of a major fault via DIP switch setting.

Logic Level Outputs (Up To Four In Any Combination)

Frequencies:	1, 5, 10 Mb/s, 8 Kb/s, 64 Kb/s, 2048 Kb/s, user configurable via jumper setting.
Interface:	Balanced, RS-422 levels into 100 Ω, on wire wrap pins, or unbalanced ACMOS levels into 50 Ω, on BNC connector, factory configured.
Alarm Control:	Outputs may be user configured to be turned off on occurrence of a major fault via DIP switch setting.

Analog Sine Outputs (Up To Four In Any Combination)

Frequencies:	1, 5, 10, 2.048 MHz, factory configured.
Interface:	Balanced, 1 V into 100 Ω, on wire wrap pins or unbalanced 1 Vrms into 50 or 75 Ω, on BNC connector, factory configured.
Alarm Control:	Outputs may be user configured to be turned off on occurrence of a major fault via DIP switch setting.

2-1 INSTALLATION

2-2 With power removed from the XL-DC, this option is physically installed by removing the two (four for double height option) screws which secure one (two for double height option) blank panel(s) on the rear of the XL-DC chassis, sliding in the 87-6000-E1 module and replacing the screws.

Prior to applying power to the XL-DC, the user configurable jumper and DIP switch settings must be made:

2-4 E1 Output Wave Shaping

	E1 Output A			E1 Output B			
S1 Position	1	2	3	4	5	6	7
Do not use	ON	ON	ON	ON	ON	ON	ON
CEPT G.703	X	X	X	X	X	X	X

Here 'X' means that the setting is not important, except that for either output, all ON is not allowed.

2-5 E1 AIS Assertion and Output Signal Control on Major Fault

Assert AIS and Turn Off Outputs: S1 Position 8 OFF
No AIS and Leave Outputs On: S1 Position 8 ON

2-6 Output Signal Frequency Selection:

Jumper Block	Output 1 J7	Output 2 J6	Output 3 J5	Output 4 J4
10 Mb/s	Pos.1	Pos.1	Pos.1	Pos.1
5 Mb/s	Pos.2	Pos.2	Pos.2	Pos.2
1 Mb/s	Pos.3	Pos.3	Pos.3	Pos.3
2048 Kb/s	Pos.4	Pos.4	Pos.4	Pos.4
8 Kb/s	Pos.5	Pos.5	Pos.5	Pos.5
64 Kb/s	Pos.6	Pos.6	Pos.6	Pos.6

* Composite Clock is a factory configured option available on Output 1.

3-1 OPERATION

3-2 No special operation procedures are required, however configuration of the Major and Minor faults via Keypad or Serial I/O Function 73 will affect the operation of this option when AIS and Output signal control is enabled via DIP switch S1, position 8. See Manual Section III for use of I/O Function 73 and for general XL-DC operation.

Note: Alarm Relay closures are silk-screened on the panel above the three wire wrap pins. These silk-screen legends indicate the *non-energized* state of the relay closures. During normal operation, the relays are *energized* so that a power failure would indicate a fault condition. Therefore the Alarm state is the *non-energized* state which is described by the silk-screened legends.

4-1 THEORY OF OPERATION

4-2 The XL-DC provides accurate time and frequency whenever one or more satellites are in view, with optimal performance when four or more satellites are in view. When satellite outages do occur, the XL-DC flywheels on its oscillator, either internal or, when using the External Oscillator Control option, external oscillator. Since the outputs from this option module are phase locked to the XL-DC internal or external 10 MHz oscillator, the accuracy and stability provided by the GPS disciplining is characteristic of these outputs as well. With the choice of a suitable oscillator option, Telecommunications Stratum I, Primary Reference Source performance is realizable from the outputs of this option module.

4-3 Refer to sheets 2, 3, and 4 of schematic drawing 86-6000 for the circuit description which follows. U7 is a Field Programmable Gate Array (FPGA) which performs these functions:

1) Interfaces to the host XL-DC 8-bit uP bus via connector P1 to obtain XL-DC status and alarm information.
2) Generates various frequencies from the XL-DC 10 MHz reference needed to create a phase detector output signal, PHI for use in PLL synthesizing the telecommunications frequencies.

3) Generates the 1 MB/S and 5 MB/S signals from the XL-DC 10 MHz reference.
4) Generates the 8 KB/S, 64 KB/S and T1E1CLK (E1, 2048 KB/S for this option) signals from the 8.192 MHz phase locked VCXO.
5) Generates the framing data stream, ALLONES for the E1 format that is needed by U8 and U9, the DS2186 Transmit Line Interface IC's.
6) Generates the Composite Clock AMI differential transformer drive signals, CCLOW, and CCHIGH
7) Controls the TAIS, ZCSEN, TCLKSEL, ALENOUT0, ALENOUT1, ALENOUT2, BLENOUT0, BLENOUT1, BLENTOUT2 signals used in configuring U8 and U9.
8) Monitors the line fault detection signals, /LFA and /LFB from U8 and U9, for generation of the summary major alarm control signal, MAJOR.
9) Controls the operation of K1 and K2, the Major and Minor Alarm Relays via signals MAJOR and MINOR.
10) Monitors the user configuration DIP switch, S1 and performs the required operations to implement the configuration.

U6 is a serial PROM which contains the configuration data for U7. This data is loaded into U7 at power up, or whenever /SYSRST is asserted.

4-4 Crystal Y1 and inverter U1:B along with varicap diode CR2, and C12, C15, and C16 comprise a Voltage Controlled Crystal Oscillator (VCXO) operating at 8.192 MHz. This VCXO is phase locked to the XL-DC 10 MHz via the loop integrator/filter comprised of U3:A and its associated passive components, which is driven by the phase detector output signal, PHI. The 8.192 MHz signal clocks FPGA U7 and is the source for the various pulse rates required for the generation of the various telecommunications outputs.

4-5 U8 and U9 in conjunction with pulse transformers T1 and T2 provide the balanced, framed E1 signals available at P3 and the optional unbalanced, framed E1 signals at J6 and J7. J6 and J7 are factory wired to BNC connectors when required. JP2 and JP3 must be closed for unbalanced operation.

4-6 Sheet 4 is the schematic of the four optional, configurable outputs. Jumper blocks, JP9, JP8, JP7, JP6, JP5, and JP4 allow selection of a desired input signal for output from OUT1, OUT2, OUT3, and OUT4, respectively. When operation is balanced, the output pairs are available at wire wrap connector P3. When operation is unbalanced, the outputs are available at J4, J2, J3, and J5. These are factory wired to BNC connectors when required.

4-7 U5 is an RS-422 driver which is present only for balanced, logic level operation. U11 is an ACMOS driver which is present only for unbalanced logic level operation and balanced or unbalanced sine wave output operation. When U11 is configured for balanced output operation, transformers T6, T5, T4, and T3 are present. Sine wave operation requires selected values present at locations L3, L4, L5, and L6 and C23, C24, C25, and C26. When unbalanced logic levels are required, these components are replaced with zero ohm resistors.

When composite clock output is configured, ACMOS driver U2 and pulse transformer T7 are present. The composite clock output signal is connected through OUT1 as a balanced signal on connector P3.

4-8 Alarm Operation--The logic resident in the FPGA, U7 implements major and minor alarm generation by monitoring two bytes broadcast once per second over the XL-DC bus by the host microprocessor residing on the GPS-XL module, and the /LFA and /LFB signals sourced by U8 and U9, which indicate E1 output line faults.

One of the two broadcast bytes gives the indication that the XL-DC is operating properly and within its specifications for time and frequency accuracy and stability. The other broadcast byte provides direct indication of major and minor alarm status of the XL-DC. The logic in the FPGA combines the line fault signals and the broadcast byte inputs to form a summary major alarm indication. The FPGA uses the broadcast byte minor alarm information verbatim to control minor alarm indication. In addition, if position 8 of S1 is in the OFF position, then the FPGA will cause U8 and U9 to transmit the AIS pattern and will turn off the optional output signals whenever a major alarm occurs.

The FPGA also implements a "watchdog" function by requiring that the broadcast bytes are in fact broadcast once a second. Should they not arrive on time, then the FPGA would assert a major alarm. This assures that failure of the main XL-DC processor would be detected.

5-1 MAINTENANCE

5-2 There is no maintenance required for this option.